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CIRCUIT DESCRIPTION		

SYMBOL TAPC UNIT CONTROLLER BOARD C

TERM. MOD.	FUNCT.	TERM.	LOC.
BACRO	I	315	342
BESPACE	I	017	486
BFIELD	I	317	480
CLB911	I	018	241
CLK921	I	118	240
CLCKRO	I	300	480
ENH01	I	207	346
FILEH01	I	003	346
PADO	I	316	481
HILVLL1	I	104	480
IN17B0	I	009	480
MAINT1	I	108	483
MOD0	I	103	485
ROBLECO	I	016	486
ROBUT1	I	208	346
REVO	I	219	481
RSF1	I	101	244
RADDSH00	I	013	480
RUWSTPC0	I	117	353
SOBTO	I	214	245
SHCRC1	I	106	345
STPC0	I	012	483
SWSTPC0	I	318	343
TTB8TO	I	302	482
TTERTAO	I	113	482
WEH8AO	I	107	345
WRITPC0	I	019	240
WRITCO	I	211	486
BLRCK0	B	001	416
BLRCK1	B	201	416
BSHPO	B	006	214
BSHMO	B	002	416
FILL0	B	303	346
FILL1	B	004	345
ROB00	B	310	249
SOH0	B	306	346
STBPP0	B	301	416
MDATA	B	312	245
HILVEL1	B	218	312
ROB01	B	109	217
STBPP0	B	209	314
MDATA	B	102	214
MD1	B	010	211
+5	P	000	214
+5	P	119	214
GRD	G	200	217
GRD	G	319	217

RECORD OF CHANGES				
CHG ISS	PREV FURN	STD	MFR D/C	SEC NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

NOTES:

- GROUND RETURN
- UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL (+PLUS)
OR -MINUS) ARE IN VOLTS

- BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

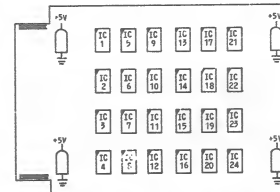
IC CODE	BAT. TERM.	GRD. TERM.
41A8	16	B
41A6	16	7,8
41B9	16	8
41CA	16	B
41CC	16	B
41CJ	16	B
41U	16	B
41W	16	B

- BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
+5	000, 119
GRD	200, 319

- HORIZONTAL MOUNTING CENTERS AT 0.50 INCH.

- INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN).



SUPPORTING INFORMATION

CATEGORY	NO.
CIRCUIT PACK CODE	JK18
CONNECTION ON FRAME	947A OR 947C
ACCEPTABLE SERIES	3

CURRENT DRAIN: 300ma

SHEET INDEX NOTES

- WHEN CHANGES ARE MADE IN THIS DRAWING ONLY THOSE SHEETS AFFECTED WILL BE REISSUED.
- THIS SHEET INDEX WILL BE REISSUED AND BROUGHT UP TO DATE EACH TIME ANY SHEET OF THE DRAWING IS REISSUED, OR A NEW SHEET IS ADDED.
- THE ISSUE NUMBER ASSIGNED TO A CHANGED OR NEW SHEET WILL BE THE SAME ISSUE NUMBER AS THAT OF THE FIRST SHEET.
- SHEETS THAT ARE NOT CHANGED WILL RETAIN THEIR EXISTING ISSUE NUMBER.
- THE LAST ISSUE NUMBER OF THE FIRST SHEET INDEX IS RECORDED AS THE LATEST ISSUE NUMBER OF THE DRAWING AS A WHOLE.

NOTICE - NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

JK18 CIRCUIT PACK
CARTRIDGE TAPE TRANSPORT CONTROLLER BOARD C
CIRCUIT

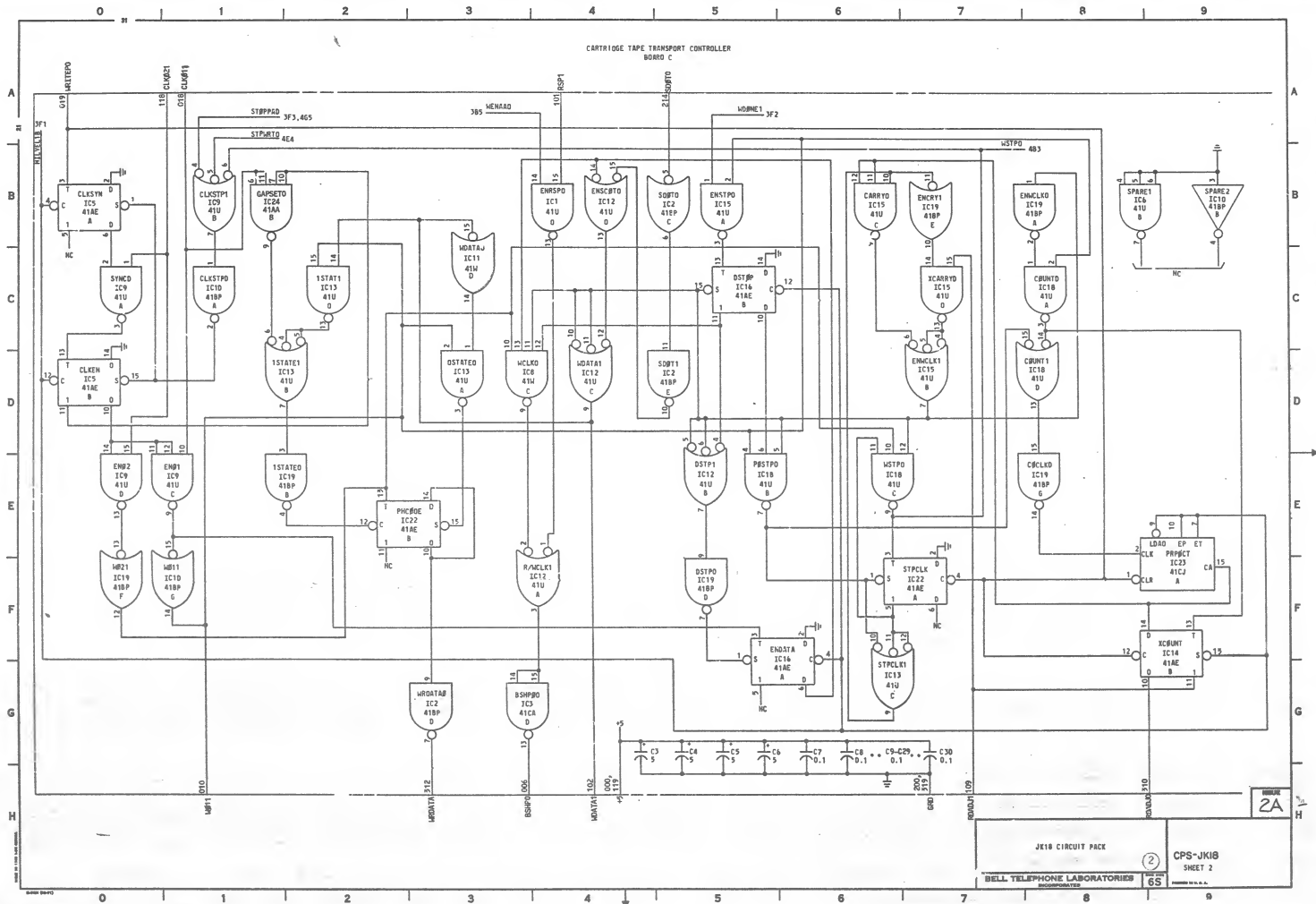
BELL TELEPHONE LABORATORIES
BELL SYSTEM

ISSUE
2A

AT&T
STANDARD

CPS-JK18
8 SHEETS

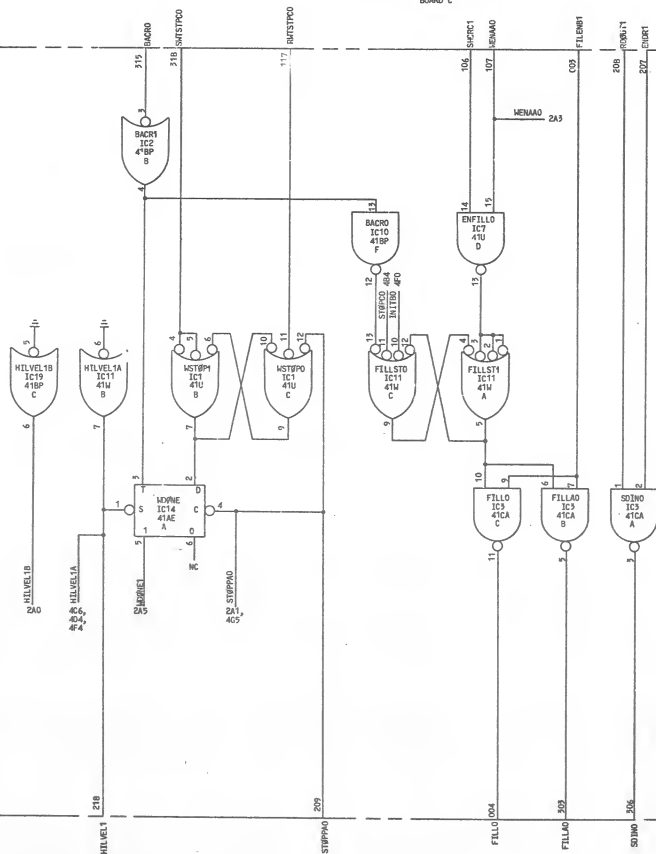
CARTRIDGE TAPE TRANSPORT CONTROLLER BOARD C



J518 CIRCUIT PACK

CPS-JK18
SHEET 2

BELL TELEPHONE LABORATORIES

CARTRIDGE TAPE TRANSPORT CONTROLLER
BOARD C

JK18 CIRCUIT PACK

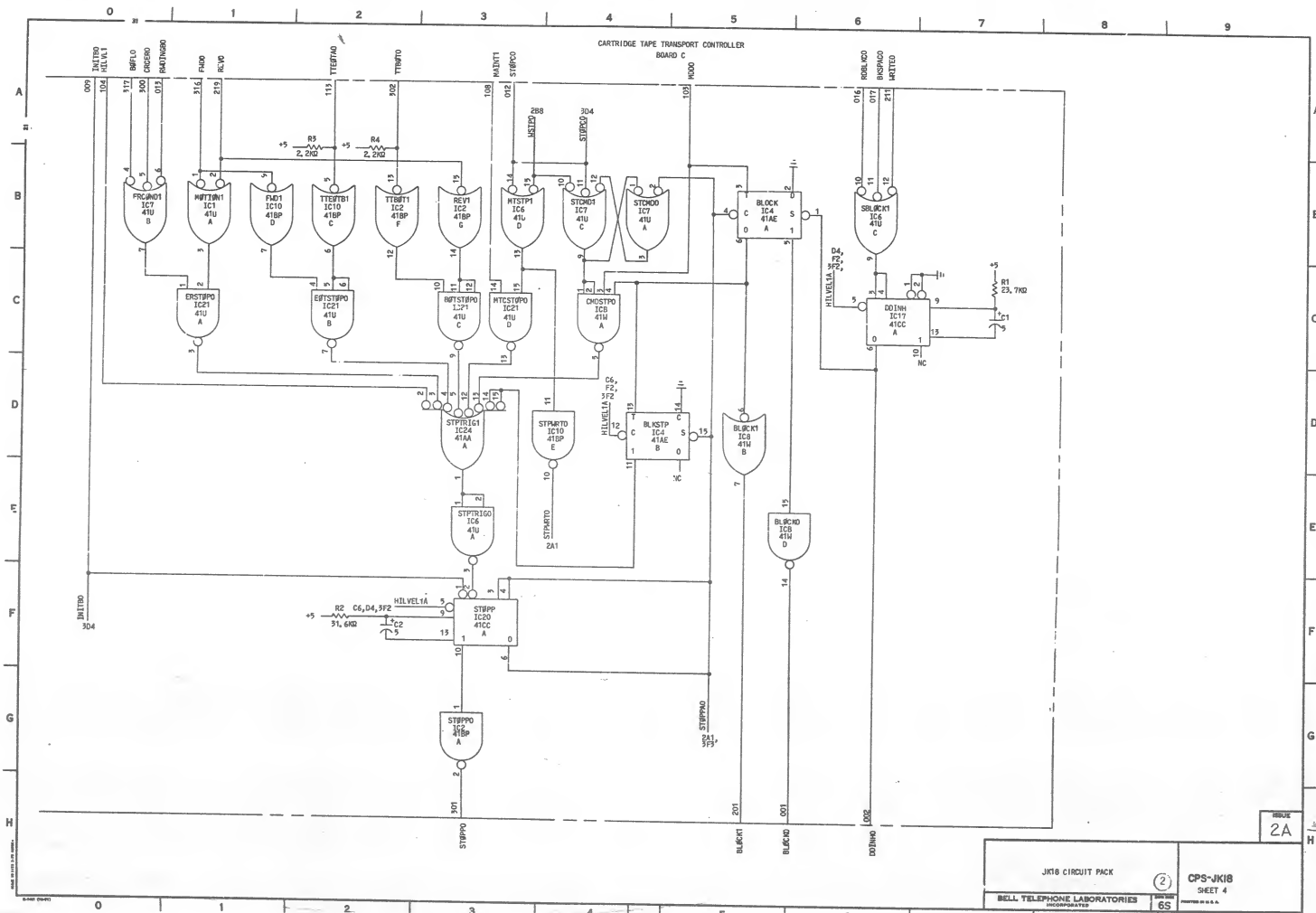
BELL TELEPHONE LABORATORIES
INCORPORATED

CPS - JK18
SHEET 3

(2)

69

69



COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 41U	IC2 41BP	IC3 41CA	IC4 41AE	IC5 41AE	IC6 41U	IC7 41U	IC8 41U	IC9 41U	IC10 41BP	IC11 41U	IC12 41U
	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	MTTBN1 481	STBPP0 481	SDNO 366	BLCKP 485	CLKS10 200	STFTB100 4E3	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
B	WSTBP1 303	WSTBP1 303	FILLAO 3E5	BLCKSTP 404	CLKEN 200	SPARE1 485	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
C	WSTBP0 284	WSTBP0 285	FILL0 3E5	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
D	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
E	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
F	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
G	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
H	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
I	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
J	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
K	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
L	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
M	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
N	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
O	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
P	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
Q	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
R	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
S	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
T	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
U	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
V	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
W	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
X	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
Y	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4
Z	WSTBP0 284	WSTBP0 285	BLCKSTP 404	BLCKSTP 404	CLKEN 200	WSTBP1 303	STCNO1 484	CMSTP0 4C4	SYNCO 2C0	CLKSTP0 2C1	FILLST1 305	RACLK1 2F4

LOC CODE ELEM ID	IC13 41U	IC14 41B	IC15 41U	IC16 41AE	IC17 41CC	IC18 41U	IC19 41BP	IC20 41CC	IC21 41U	IC22 41AE	IC23 41CJ	IC24 41AA
A	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
B	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
C	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
D	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
E	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
F	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	
G	OSTATED 203		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303		WSTBP1 303	

CAPACITOR

DESIG	CODE
61C1-C6	601A,5
241C7-C30	KS-19774 LS,0,1

RESISTOR

DESIG	CODE
R1	KS-20616 L16,23,700
R2	KS-20616 L16,31,600
R3	KS-20616 L16,2,200
R4	KS-20616 L16,2,200

JK18 CIRCUIT PAGE

BELL TELEPHONE LABORATORIES

CPS-JK18

SHEET 5

REVISED 10-6-64

2A

CIRCUIT DESCRIPTION

A. FUNCTIONAL DESCRIPTION

JK18 IS ONE OF THE FOUR CARTRIDGE TAPE TRANSPORT CONTROLLER (CTTC) BOARDS. IT CONTAINS THE WRITE CARRY, COMMAND, STOP LOGIC, AND BUFFER FILL REQUEST CIRCUITRY. THE WRITE CIRCUITRY INCLUDES A PREamble GENERATOR, A POSTamble GENERATOR, AND A DATA PHASE ENCODER CIRCUIT.

FIGURE 1 IS A BLOCK DIAGRAM OF JK18. AS A WRITE OPERATION BEGINS, A 40ms PULSE OCCURS ON THE WRITE START PULSE INPUT LEAD. THIS PULSE, WHICH COMES FROM THE WRITE DATA CARRY CIRCUT LOCATED ON JK19, IS INITIATED BY A WRITE COMMAND FROM THE CTTC. THE CARTRIDGE TAPE TRANSPORT (CTT) BEGINS TO MOVE FORWARD AT READ-WRITE LEAD AS THE COMMAND IS ISSUED. THE CLOCK SYNC CIRCUIT, WHICH HAS LEFT IN A DISABLED STATE FROM THE PREVIOUS WRITE OPERATION OR INITIALIZATION SEQUENCE, WILL MAINTAIN AN INTERIOR BLOCK GAP (IBG) STATE AT THE OUTPUT OF THE PHASE ENCODER CIRCUIT UNTIL THE TRAILING EDGE OF THE WRITE-START PULSE. THIS STATE MAINTAINS A CONSTANT LOW LEVEL AT THE CLOCK INPUTS OF THE PHASE ENCODER CIRCUIT, WHILE THE CTT IS WRITE ENABLED AND MOVING FORWARD AT READ-WRITE LEAD. IT WILL EFFECTIVELY WRITE AN IBG ONTO THAT PORTION OF TAPE WHICH PASSES THE WRITE JING ONTO THAT PORTION OF TAPE. THE TRAILING EDGE OF THE WRITE START PULSE ENABLES THE CLOCK SYNC CIRCUIT. THIS CIRCUIT WILL THEN SYNC IN ON THE TWO CLOCK SIGNALS APPEARING ON THE CARRY AND CLOCK INPUTS. CARRY AND CLOCK (ONE UP A SINGLE 2-PHASE CLOCK OPERATING AT 48 KHz) ARE GENERATED BY A CRYSTAL OSCILLATOR CIRCUIT LOCATED ON JK19. 2011H CLOCK SIGNALS PROVIDE 5μs PULSES THAT ARE 180° OUT OF PHASE WITH EACH OTHER. THE SYNC CIRCUIT ALSO ENSURES THAT THE FIRST CLOCK PULSE AT ITS OUTPUT WILL APPEAR ON P1.

THE 2-PHASE CLOCK AT THE OUTPUT OF THE SYNC CIRCUIT FEEDS THE PHASE ENCODER CIRCUIT AND THE PREamble/POSTamble GENERATOR CIRCUIT. THE PHASE ENCODER CIRCUIT RECEIVES DATA FROM THE DATA SELECTOR CIRCUIT, AND BY UTILIZING THE 2-PHASE CLOCK, IT WILL TRANSLATE ANY NONZERO TO ZERO (NRZ) DATA, APPEARING AT THE OUTPUT DATA SELECTOR, TO THE ENCODED (PE) DATA. THE PE DATA LEAD IS FED DIRECTLY TO THE CTT'S WRITE CIRCUITS.

THE PREamble/POSTamble GENERATOR PROVIDES DATA TO THE DATA SELECTOR CIRCUIT FOR WRITING THE PREamble (12 ZEROS FOLLOWED BY A SINGLE ONE) AND THE POSTamble (A SINGLE ONE FOLLOWED BY 12 ZEROS). IT ALSO PROVIDES CONTROL TO THE DATA SELECTOR AND THE BUFFER CLOCK LEAD (DATA IN) FROM THE PHASE ENCODER CIRCUIT IS INITIALLY ENABLED, THE DATA ENABLE LEAD WILL BE IN A STATE SUCH THAT DATA AT THE OUTPUT OF THE PREamble/POSTamble GENERATOR WILL BE GATED THROUGH THE DATA SELECTOR. THE CLOCK OUTPUT OF THE PREamble/POSTamble GENERATOR CIRCUIT IS DISABLED FOR THE FIRST 15 CYCLES OF THE 2-PHASE CLOCK. THE DATA OUTPUT OF THE PREamble/POSTamble GENERATOR WILL REMAIN IN THE "ZERO" STATE. THIS OUTPUT GOES TO A "ONE" STATE FOR THE NEXT 15 CYCLES OF THE 2-PHASE CLOCK. THIS ACCOMPLISHES WRITING OF THE PREamble ONTO TAPE. THE BUFFER CLOCK LEAD (DATA IN) IN CLOCK IS ENABLED PRIOR TO THE SIXTEENTH CYCLE OF THE 2-PHASE CLOCK; ALLOWING THE FIRST DATA BIT FROM THE BUFFER CIRCUITS TO BE LOADED ONTO THE INPUT DATA LEAD (INPUT DATA). AS THE LAST BIT OF THE PREamble IS WRITTEN ONTO TAPE, AT THIS POINT, THE DATA-ENABLE LEAD CHANGES STATES; ALLOWING DATA FROM THE BUFFER CIRCUITS TO BE GATED THROUGH THE DATA SELECTOR TO THE PHASE ENCODER CIRCUITS.

A WRITE CYCLE CAN ONLY BE ORDERED AS THE LAST DATA BIT FROM A GIVEN BUFFER IS CARRIED BY THE BUFFER CIRCUIT. THE BUFFER CARRY PULSE LEAD TO THE BUFFER CARRY PULSE LEAD. THIS PULSE WILL OCCUR EVERY 1024 BITS UNLESS THE REGISTER IS STOPPED. THEREFORE, PRESETTING THE BUFFER CARRY TO END A WRITE CYCLE, A SET WRITE STOP COMMAND IS ISSUED TO THE CTT. THIS COMMAND INITIATES A PULSE AT THE OUTPUT OF THE CTT'S COMMAND DECODER LOCATED ON JK15, WHICH APPEARS AS THE WRITE-START PULSE. THIS PULSE SETS THE WRITE-STOP LATCH, ALLOWING THE BUFFER CARRY PULSE LEAD TO THE PHASE ENCODER CIRCUIT. AT THIS POINT, ALL DATA HAS BEEN WRITTEN AND THE BUFFER-CLOCK LEAD IS DISABLED. THE DATA ENABLE LEAD SWITCHES BACK TO ITS ORIGINAL STATE, ENABLING A DATA PATH FROM THE PREamble/POSTamble GENERATOR THROUGH THE DATA SELECTOR. THE DATA LEAD OF THE PREamble/POSTamble GENERATOR IS RETURNED TO THE "ONE" STATE FROM THE LAST BIT OF THE PREamble.

IT STAYS IN THIS STATE THROUGH THE NEXT CYCLE OF THE 2-PHASE CLOCK, WHILE WRITING THE FIRST BIT OF THE POSTamble. A "ONE" STATE LEAD THEN GOES TO THE "ZERO" STATE ALLOWING THE 15 "ZEROS" OF THE POSTamble TO BE WRITTEN. THE CLOCK SYNC CIRCUIT IS THEN DISABLED, LATCHING THE PHASE ENCODER CIRCUIT IN THE "IBG" STATE. THE ACTUAL STOP SIGNAL TO THE CTT IS INITIATED BY THE READ CIRCUIT, AFTER THE READ WINDING OF THE CTT'S HEAD HAS REACHED THE IBG.

THE WRITE DATA OUTPUT (WRITE DATA) FROM THE DATA SELECTOR AND P1 (WRITE CLOCK OUTPUT LEAD) IS CONNECTED TO THE READ CIRCUIT LOCATED ON JK17. THE WRITE DATA LEAD IS THE NRZ FORM OF THE DATA BEING WRITTEN ONTO TAPE. A PULSE APPEARS ON THE WRITE CLOCK LEAD AT THE CENTER OF EACH BIT. WHEN THE CTT IS IN THE MAINTENANCE MODE, AND THE READ AND WRITE CIRCUITS ARE DISABLED WITHOUT OPERATING THE CTT, THE WRITE DATA AND WRITE CLOCK SIGNALS ARE GATED THROUGH THE READ CIRCUIT. THEREBY, TESTING ALL OF THE WRITE CIRCUITS EXCEPT THE PHASE ENCODER BY UTILIZING THE CRC CIRCUIT LOCATED ON JK17.

THE STOP CIRCUIT OPERATES A 40ms STOP PULSE WHENEVER THE TAPE DATA CONTROLLER (CCTC) UNIT EXPERIENCES ANY OF SEVERAL CONDITIONS. THIS PULSE, WHICH APPEARS ON THE STOP PULSE LEAD, RESETS ALL CIRCUITS OF THE CTT TO THEIR INITIAL STATE. THIS STOP PULSE IS GENERATED UNDER THE FOLLOWING CONDITIONS:

- BUFFER OVERFLOW**
THE BUFFER CIRCUITS WERE NOT PROPERLY SERVICED BY THE CENTRAL PROCESSOR (ERROR CONDITION).
- CRC ERROR**
A CRC ERROR WAS DETECTED DURING THE PREVIOUS READ OR READ-AFTER-WRITE OPERATION.
- REWINDING**
THE CTT STARTS A REWIND SEQUENCE.
- BEGINNING OR END OF TAPE**
THE CTT SENSES THE PHYSICAL BEGINNING OF TAPE OR THE PHYSICAL END OF TAPE MARKERS.
- STOP**
A STOP COMMAND IS ISSUED TO THE CTT.
- THE COMPLETION OF A BACKSPACE, WRITE, OR READ-A-BLOCK OPERATION**
EITHER OF THESE COMMANDS ISSUED TO THE CTT WILL SET THE END-STOP CIRCUIT. THIS CIRCUIT MONITORS THE DATA DETECT INPUT. AFTER OBSERVING DATA DETECT GO ACTIVE, WHEN INACTIVE (INDICATING THAT THE CTT HAS CROSSED A BLOCK OF DATA) IT TRIGGERS THE STOP CIRCUIT.
- TDC INITIALIZE**
A TDC INITIALIZE COMMAND IS ISSUED TO THE TDC.

ALL READ OR SHIFT CRC (SHIFT THE CONTENTS OF THE CRC REGISTER, LOCATED ON JK17, TO THE BUFFER CIRCUITS) OPERATIONS MUST LEAVE THE ON-LINE BUFFER IN A FULL STATE. THE BUFFER CIRCUITS (ON JK19) CONTAIN THE 1024-BIT SHIFT REGISTER. THE ON-LINE BUFFER IS THE 1024-BIT SHIFT REGISTER WHICH IS ACTIVELY ACCEPTING DATA FROM OR TRANSMITTING DATA TO THE CTT. IF THE DATA TRANSMITTER TO THE BUFFER CIRCUITS IS NOT AN INCIDENT OF 1024 BITS, FROM REQUESTING DATA TO THE BUFFER CIRCUITS, THE FILL CIRCUIT INDICATES IF A FILL REQUEST SHOULD BE SENT TO THE BUFFER CIRCUITS AT THE COMPLETION OF A DATA TRANSFER SEQUENCE. THE READ-DATA CLOCK LEAD IS THE BUFFER CARRY OUTPUT FROM THE READ CIRCUIT (JK17). EACH PULSE ON THIS LEAD ATTEMPTS TO SET THE FILL REQUEST REQUEST CIRCUIT. NOTE THAT THE BUFFER-CARRY PULSE OCCURS AT THE TRAILING EDGE OF READ-DATA CLOCK PULSES. IT OCCURS ONCE EVERY 1024 CLOCK PULSES TO INDICATE THAT A COMPLETE BUFFER HAS BEEN FILLED. THE FILL REQUEST CIRCUIT WILL BE LEFT IN ITS CLEARED STATE, ONLY IF THE ON-LINE BUFFER IS FULL WHEN THE LAST DATA BIT IS LOADED ONTO IT. IF THE ON-LINE BUFFER IS NOT FULL AFTER THE LAST DATA HAS BEEN TRANSFERRED, THE FILL REQUEST CIRCUIT WILL BE LEFT IN THE ENABLED STATE. THIS CAUSES THE FILL LEAD (FILL) TO GO ACTIVE, REQUESTING THE BUFFER FILL OPERATION WHEN IT IS ENABLED BY THE FILL-ENABLE LEAD. THE FILL-ENABLE LEAD IS DRIVEN ACTIVE BY THE READ CIRCUIT AS IT COMPLETES ITS OPERATION FOR A GIVEN DATA TRANSFER FUNCTION.

THE READ DATA INPUT LEAD (THE DATA OUTPUT FROM THE READ CIRCUIT), IS ENABLED BY THE READ-DATA ENABLE LEAD TO DRIVE THE

READ OUTPUT DATA LEAD. THE READ OUTPUT DATA LEAD TRANSMITS READ DATA TO THE BUFFER CIRCUITS. THE READ DATA LEAD IS ENABLED BY JK16 WHENEVER DATA IS BEING TRANSFERRED THROUGH THE READ CIRCUITS OR FROM THE CRC REGISTER TO THE BUFFER CIRCUIT.

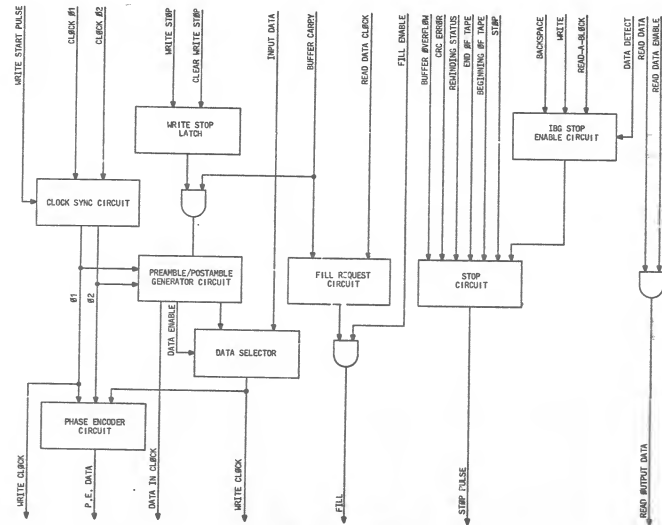


FIGURE 1 - BLOCK DIAGRAM

JK18 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

CPS-JK18
SHEET 6

1000

TO WRITE THE FIFTEENTH "ZERO" ONTO TAPE.

[illegible]

Figure 6

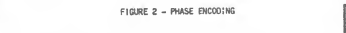
[illegible]

FIGURE 2 - FIVE-STEP PROCESS

SHEET 7

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SHEET 7

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